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CLAIMS

What is claimed is:

1	1. A method including:	
2	detecting a power management event in a system; and	
3	dynamically adjusting, in response to the power manage	ement event,
4	the performance states of a plurality of system components inclu	ıding system
5	buses.	

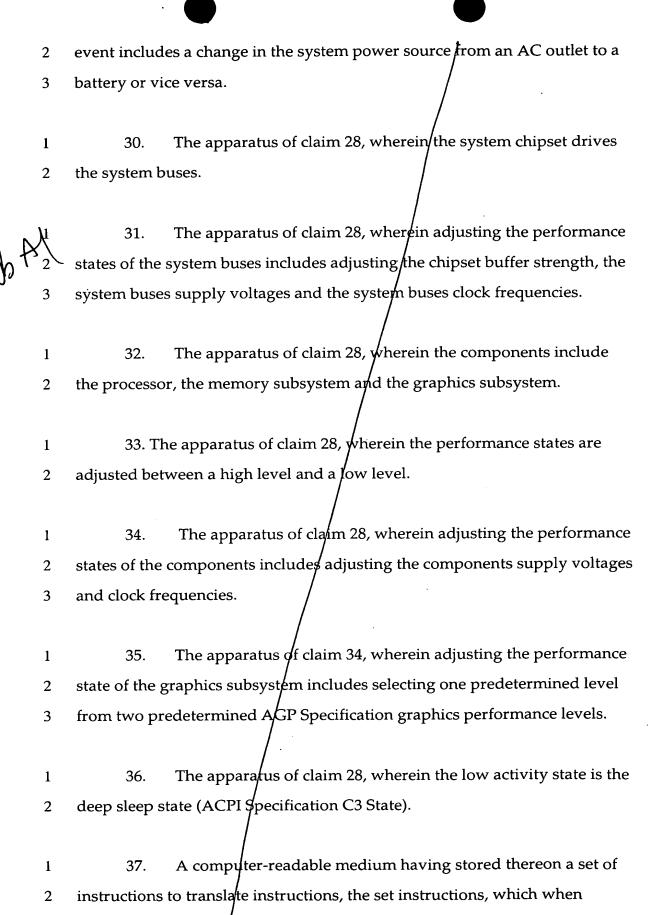
- 2. The method of claim 1, wherein the power management event includes a change in the system power source from an AC outlet to a battery or vice versa.
- 3. The method of claim 1, wherein the system chipset drives the system buses.
- 4. The method of claim 1, wherein adjusting the performance states of the system buses includes adjusting the chipset buffer strength, the system buses supply voltages and the system buses clock frequencies.
- 5. The method of claim 1, wherein the components include the memory subsystem, the graphics subsystem and the processor.
 - 6. The method of claim 1, wherein the performance states are adjusted between a high level and a low level.
- 7. The method of claim 1, wherein adjusting the performance states of the components includes adjusting the components supply voltages and clock frequencies.

1	8.	The method of claim 7, wherein djusting the performance			
2	state of the g	state of the graphics subsystem includes selecting one predetermined level			
3	from two pr	edetermined AGP Specification graphics performance levels.			
1	9.	The method of claim 1, wherein dynamically adjusting the			
2	performance	e states includes automatically placing the system in the deep			
3	sleep state (ACPI Specification C3 state) upon the occurrence of the power				
4	management event to adjust the performance states of the system				
5	components				
1	10.	A method including:			
2	detecting a power management event in a system; and				
3	automatically placing the system in a low activity state, in response to				
4	the power management event,				
5	adjusting the performance states of a plurality of system buses, and				
6	adjusting th	e performance states of a plurality of system components.			
1	11.	The method of claim 10, wherein the power management event			
2	includes a cl	hange in the system power source from an AC outlet to a battery			
3	or vice versa				
1	12.	The method of claim 10, wherein the system chipset drives the			
2	system buses.				
1	13.	The method of claim 10, wherein adjusting the performance			
2	states of the	system buses includes adjusting the chipset buffer strength, the			
3	system buse	es supply voltages and the system buses clock frequencies.			
1	14.	The method of claim 10, wherein the components include the			

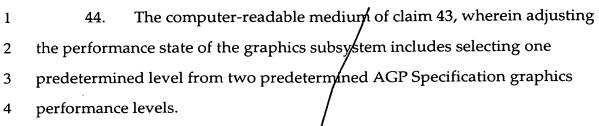
system buses.

2	processor,	the memory subsystem and the graphics subsystem.
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1	15.	The method of claim 10, wherein the performance states are
2	adjusted be	etween a high level and low level.
1	16.	The method of claim 10, wherein adjusting the performance
2	state of the	components includes adjusting the components supply voltages
3	and clock frequencies.	
1	17.	The methods of claim 16, wherein adjusting the performance
2		graphics subsystem includes selecting one predetermined level
3	from two p	redetermined AGP Specification graphics performance levels.
1	18.	The method of claim 15, wherein the low activity state is the
2	deep sleep	state (ACVI Specification C3 State).
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P11	19.	A system comprising:
2		a detector adapted to detect generation of a power
3	manageme	nt event; and
4		a controller to automatically adjust, in response to the power
5	manageme	nt event, the performance states of a plurality of system
6	components including system buses.	
	-	
1	20.	The system of claim 19, wherein the power of management
2		des a change in the system power source from an AC outlet to a
3	battery or v	vice versa.
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1	21.	The system of claim 19, wherein the system chipset drives the

1	22.	The system of claim 19, wherein adjusting the performance
2	states of the	system buses includes adjusting the chipset buffer strength, the
3	system buse	es supply voltages and the system buses clock frequencies.
1	23.	The system of claim 19, wherein the components include the
2	processor, the	he memory subsystem and the graphics subsystem.
λ_1	24.	The system of claim 19, wherein the performance states are
2	adjusted be	tween a high level and a low level.
1	25	The contains of eleies 10 subtrains directing the performance
1	25.	The system of claim 19, wherein adjusting the performance
2	states of the components includes adjusting the components supply voltages	
3	and clock fr	equencies.
1	26.	The system of claim 25, wherein adjusting the performance
2	state of the	graphics subsystem includes selecting one predetermined level
3	from two pi	redetermined AGP Specification graphics performance levels.
1	27.	The system of claim 19, wherein the low activity state is the
2	deep sleep s	state (ACPI Specification C3 State).
1	28.	An apparatus comprising:
2		a detector adapted to detect generation of power
3	managemer	nt event; and
4		a controller to automatically adjust, in response to the power
5	managemer	nt event, the performance states of a plurality of system
6	components	s including system buses.
1	29.	The apparatus of claim 28, wherein the power of management



3	executed by a processor, cause the processor to perform a method
4	comprising:
5	detecting a power management event in a system; and
6	dynamically adjusting, in response to the power management
7	event, the performance states of a plurality of system components including
8	system buses.
1	38. The computer-readable medium of claim 37, wherein the
2	power management event includes a change in the system power source
3	from an AC outlet to a battery or vice versa
1	39. The computer-readable medium of claim 37, wherein the
2	chipset drives the system buses.
1	40. The computer-readable medium of claim 37, wherein adjusting
2	the performance states of the system buses includes adjusting the chipset
3	buffer strength, the system buses supply voltages and the system buses clock
4	frequencies.
1	41. The computer-readable medium of claim 37, wherein the
2	components include the memory subsystem, the graphics subsystem and the
3	processor.
1	42. The computer readable medium of claim 37, wherein the
2	performance states are adjusted between a high level and a low level.
1	43. The computer-readable medium of claim 37, wherein adjusting
2	the performance states of the components includes adjusting the
3	components supply voltages and clock frequencies.
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45. The computer-readable medium of claim 37, wherein dynamically adjusting the performance states includes automatically placing the system in the deep sleep state (ACPI Specification C3 State) upon the occurrence of the power management event to adjust the performance states of the system components.